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(54) Process of removing polymers in semiconductor vias

Verfahren zur Entfernung von Polymeren aus Sacklöchern in Halbleitervorrichtungen

Procédé d'élimination de polymères de trous borgus dans des dispositifs semi-conducteurs

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Description

The present invention relates generally to semiconductor integrated circuits, and more specifically to the formation of contact vias in an integrated circuit.

In semiconductor integrated circuits, formation of interconnect layers is important to the proper operation of these devices. Interconnect signal lines make contact with lower conductive layers in the integrated circuit through vias in an insulating layer. For best operation of the device, the lower conductive layers should not be damaged during formation of the contact via.

Various interlevel insulating layers are deposited on the integrated circuit during formation of the device. These layers separate the conductive layers from each other. One method to form contact vias through these insulating layers utilizes a resist layer to define the via locations. An anisotropic etch is then performed to open the vias. During the anisotropic etch, however, polymers are created from the resist and the etch chemistry, and. adhere to the sidewalls of the via. These polymers need to be removed so that proper contact is made in the via between the conductive layers.

As known in the prior art, the polymers are removed or dissolved through the use of a solvent, acid or plasma etch. During this process, however, a substantial amount of the underlying aluminum conductive layer can be removed. Additionally, the acid or plasma etch can remove some of the insulating layer, which enlarges the size of the via. A complete study about the nature of these polymers was published by D. Allred et al. in Journal of Vacuum Science and Technology B, vol.7, no.3, 1989, pages 505-511.

Therefore, it would be desirable to provide a technique for forming contact vias in integrated circuits without damaging the underlying conductive layers or enlarging the size of the via.

It is therefore an object of the present invention to provide a method for forming contact vias in an integrated circuit without damaging underlying conductive layers.

It is another object of the present invention to provide a method for forming contact vias wherein the shape and size of the vias are not altered.

It is another object of the present invention to provide such a method and structure which is compatible with standard process flows, and which add minimal additional complexity to the fabrication of a typical integrated circuit.

According to claim 1 of the present invention there is provided a method for forming a via, comprising the steps of forming an oxide layer over a conductive element; forming and patterning a resist layer over the oxide layer to define via locations; anisotropically etching the oxide layer to open vias in the via locations, characterised by removing contaminate particles created from the resist and etch chemistry, containing a polymer and formed on the sidewalls of the via with a chemical which acts as a developer for the resist.

As described, a method for forming a contact via in an integrated circuit includes the formation of an aluminum conductive element on an integrated circuit device. A conformal insulating layer is then deposited over the device. Using a masking layer, an anisotropic etch is performed to open a via through the conformal insulating layer. During the anisotropic etch, polymers are created from the resist and etch chemistry and adhere to the sidewalls of the via. A resist developer containing tetra methyl ammonium hydroxide is used to remove the polymers from the via. A contact may now be formed by depositing conductive material into the via.

A resist developer containing tetra methyl ammonium hydroxide is known from JP-A-6 400 2325, Database WPIL, Section Ch, Week 0789, Derwent Publications Ltd, London, GB, Class G.

The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself however, as well as a preferred mode of use, and further objects and advantages thereof, will best be understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein:

Figures 1 and **2** are sectional views illustrating a prior art method for forming a via in an integrated circuit; and

Figures 3 - 5 are sectional views illustrating the preferred method for forming a via in an integrated circuit according to the present invention.

The process steps and structures described below do not form a complete process flow for manufacturing integrated circuits. The present invention can be practiced in conjunction with integrated circuit fabrication techniques currently used in the art, and only so much of the commonly practiced process steps are included as are necessary for an understanding of the present invention. The figures representing cross-sections of portions of an integrated circuit during fabrication are not drawn to scale, but instead are drawn so as to illustrate the important features of the invention.

Figures 1 and **2** depict formation of an interlevel contact via as known in the prior art. Referring to **Figure 1**, a conductive element **10** is formed on an interlevel insulating layer **12**. The conductive element **10** is made from aluminum, and the insulating layer **12** may be made from oxide. A conformal insulating layer **14** of oxide is then deposited over the device. Using a masking layer (not shown), an anisotropic etch is performed to open a via **16** through the conformal insulating layer **14**. During the anisotropic etch, polymers **18** are formed from the resist and etch chemistry. These polymers **18** adhere to the sidewalls of the via **16**.

Figure 2 illustrates the via after the polymers **18** have been removed. Typically, a plasma etch or a sol-

vent known in the art as piranha, which contains a mixture of hydrogen peroxide and sulfuric acid, is used to remove the polymers **18**. One skilled in the art will recognize that piranha will not damage an underlying conductive layer made from polycrystalline silicon. If, however, the underlying conductive layer is made from aluminum, a refractory metal, or a silicided poly, piranha will etch into the material, and can remove a substantial amount of the layer. Thus, the acid used to remove the polymers **18** creates undesirable holes in the aluminum.

If a plasma etch is used to remove the polymers **18**, undesirable holes can also be formed in the aluminum due to the overetching required to ensure complete removal of the polymers **18**. If the etch is not performed long enough, some of the polymers **18** will not be removed. Thus, a plasma etch presents a trade off. Either holes are formed in the aluminum or not all of the polymers **18** are removed.

Another problem encountered with this method is the plasma etch or acid also removes some of the conformal insulating layer **14**. This increases the size of the via **16**, and smooths out the sidewalls of the via **16**. Increasing the size of the via **16** can ultimately result in decreasing the total number of components that can be built on the integrated circuit.

Figures 3 - 5 illustrate the formation of vias according to the present invention. Referring to **Figure 3**, a conductive element **20** is formed on an interlevel insulating layer **22**. A conformal insulating layer **24** is deposited over the device. The conductive element **20** is made from aluminum, and the insulating layers may be made from oxide. Using a masking layer (not shown), an anisotropic etch is performed to open a via **26** in the conformal insulating layer **24**. During the anisotropic etch, polymers **28** are formed from the resist and etch chemistry. These polymers **28** adhere to the sidewalls of the via **26**.

Figure 4 illustrates a device after the polymers **28** have been removed. A resist developer containing Tetra Methyl Amonium Hydroxide (TMAH) is used to remove the polymers **28** in the via **26**. One resist developer which can be used, for example, is sold under the brand name of Microposit Developer S-319, and is manufactured by Shipley Co., Inc. By using a resist developer containing TMAH, the size and sidewalls of the via are not affected. Thus, via does not enlarge, and sidewalls are left rough. Additionally, a relatively small portion of the aluminum is removed.

Referring to **Figure 5**, a conductive layer **30** is deposited over the device and extends into the via **26**, forming a conductive contact between the aluminum and the conductive layer **30**. The integrated circuit is now ready for further processing using techniques which are known in the art.

It will be appreciated by those skilled in the art, the techniques described above create vias without removing a substantial amount of aluminum. Additionally, the resist developer used to remove the polymers does not etch oxide, thereby maintaining the desired size of the via.

While the invention has been particularly shown and described with reference to a preferred embodiment, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the scope of the invention as defined by the appended claims.

Claims

1. A method of forming a via, comprising the steps of:
   forming an oxide layer (20) over a conductive element (20) ;

   forming and patterning a resist layer over the oxide layer to define via locations;
   anisotropically etching the oxide layer to open vias (26) in the via locations,
   removing with a chemical contaminate particles created from the resist and etch chemistry, said particles containing a polymer and being formed on the sidewalls of the via, characterised in that said chemical acts as a developer for the resist.

2. The method of claim 1 wherein the conductive element comprises aluminum.

3. The method of claim 1 wherein the conductive element comprises a refractory metal.

4. The method of claim 1, wherein said resist layer comprises a positive resist.

5. The method of any preceding claim, wherein said chemical contains Tetra Methyl Amonium Hydroxide.

6. The method of any preceding claim, wherein a conductive layer (30) is deposited over the device after the contaminate particles are removed, wherein a conductive contact is made between the conductive element and the conductive layer.

Patentansprüche

1. Verfahren zur Ausbildung eines Loches bzw. Durchgangsloches mit den Schritten:

   eine Oxidschicht (20) wird über einem leitenden Element (20) ausgebildet;
   eine Resist- bzw. Photolackschicht wird über der Oxidschicht ausgebildet und strukturiert bzw. mit einem Muster versehen, um Loch- bzw. Durchgangslochplätze festzulegen;

die Oxidschicht wird anisotrop geätzt, um Löcher bzw. Durchgangslöcher (26) in den Lochbzw. Durchgangslochplätzen zu öffnen, Kontaminierungs- bzw. Schmutzteilchen, die durch die Resist- bzw. Photolack- und Ätzchemie erzeugt worden sind, werden mit einer Chemikalie entfernt, wobei die Teilchen ein Polymer enthalten und auf den Seitenwänden der Löcher bzw. Durchgangslöcher ausgebildet sind, dadurch **gekennzeichnet**, daß die Chemikalie für den Resist bzw. Photolack als ein Entwickler wirkt.

2. Verfahren nach Anspruch 1, bei dem das leitende Element Aluminium aufweist.

3. Verfahren nach Anspruch 1, bei dem das leitende Element ein hochwiderstandsfähiges bzw. hochschmelzendes Metall aufweist.

4. Verfahren nach Anspruch 1, bei dem die Resist- bzw. Photolackschicht einen positiven Resist bzw. Photolack aufweist.

5. Verfahren nach einem der voranstehenden Ansprüche, bei dem die Chemikalie Tetramethylammoniumhydroxid enthält.

6. Verfahren nach einem der voranstehenden Ansprüche, bei dem eine leitende Schicht (30) über der Einrichtung abgeschieden wird, nachdem die Kontaminierungs- bzw. Schmutzteilchen entfernt worden sind, wobei ein leitender Kontakt zwischen dem leitenden Element und der leitenden Schicht hergestellt wird.

Revendications

1. Procédé de formation d'un via, comprenant les étapes consistant à :

former une couche d'oxyde (24) sur un élément conducteur (20) ;
former et graver une couche de résine sur la couche d'oxyde pour définir des emplacements de vias ;
graver de manière anisotrope la couche d'oxyde pour ouvrir des vias (26) dans les emplacements de vias ;
éliminer avec un agent chimique des particules contaminantes formées à partir de la résine et des produits de gravure, ces particules contenant un polymère et étant formées sur les parois latérales du via,

caractérisé en ce que ledit agent chimique agit comme développeur pour la résine.

2. Procédé selon la revendication 1, dans lequel l'élément conducteur comprend de l'aluminium.

3. Procédé selon la revendication 1, dans lequel l'élément conducteur comprend un métal réfractaire.

4. Procédé selon la revendication 1, dans lequel la couche de résine comprend une résine positive.

5. Procédé selon l'une quelconque des revendications précédentes, dans lequel l'agent chimique contient du tétraméthylhydroxyde d'ammonium.

6. Procédé selon l'une quelconque des revendications précédentes, dans lequel une couche conductrice (30) est déposée sur le dispositif après l'élimination des particules contaminantes, et dans lequel un contact conducteur est réalisé entre l'élément conducteur et la couche conductrice.

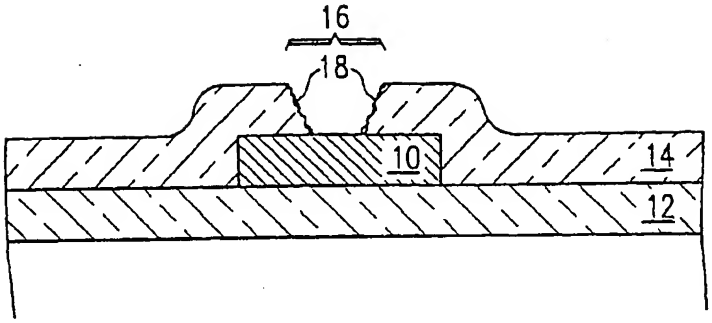

FIG. 1
(PRIOR ART)

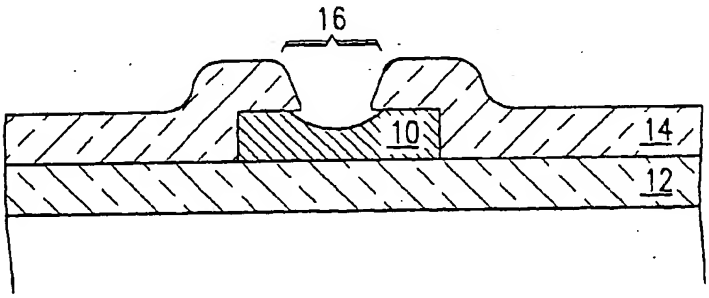

FIG. 2
(PRIOR ART)

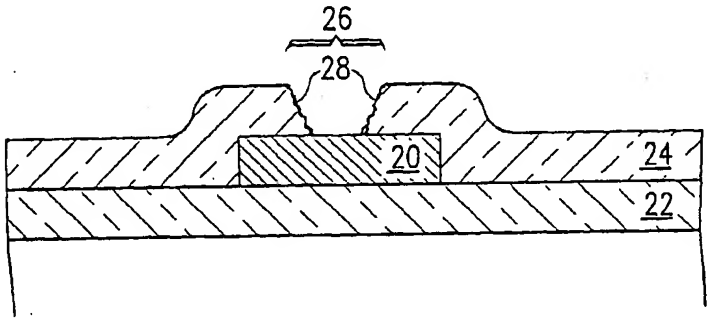

FIG. 3

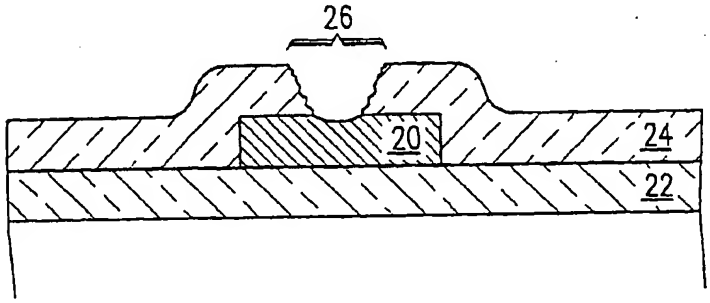

FIG. 4

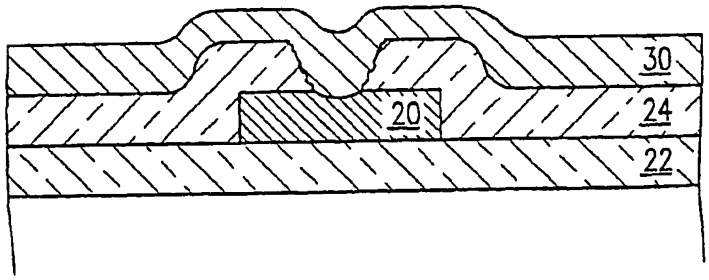

FIG. 5